Title: CREATING OPTIMIZED PHYSICAL IMPLEMENTATIONS FROM HIGH-LEVEL DESCRIPTIONS OF ELECTRONIC DESIGN USING PLACEMENT-BASED INFORMATION

Inventor: Tommy K. Eng

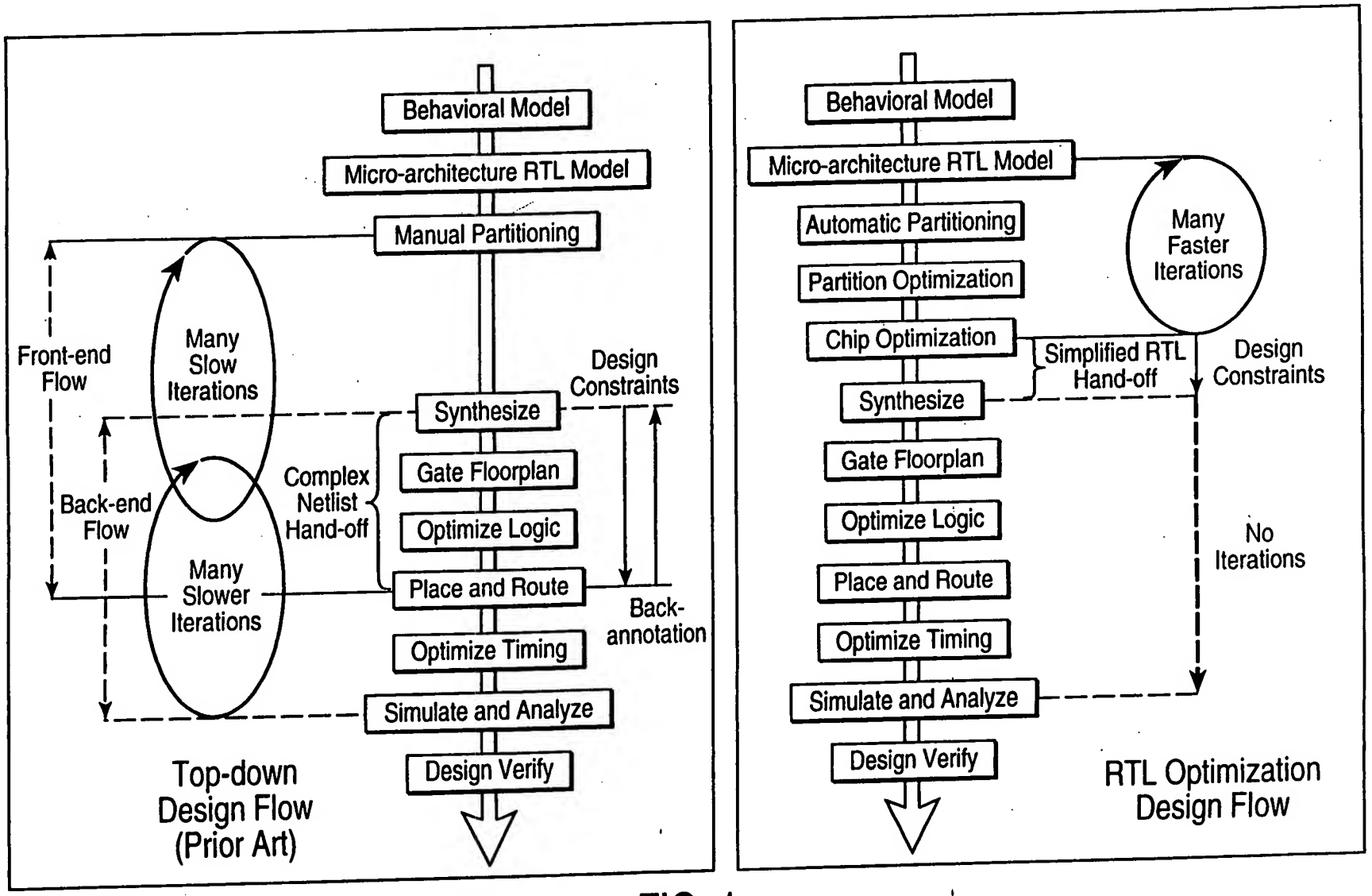


FIG. 1

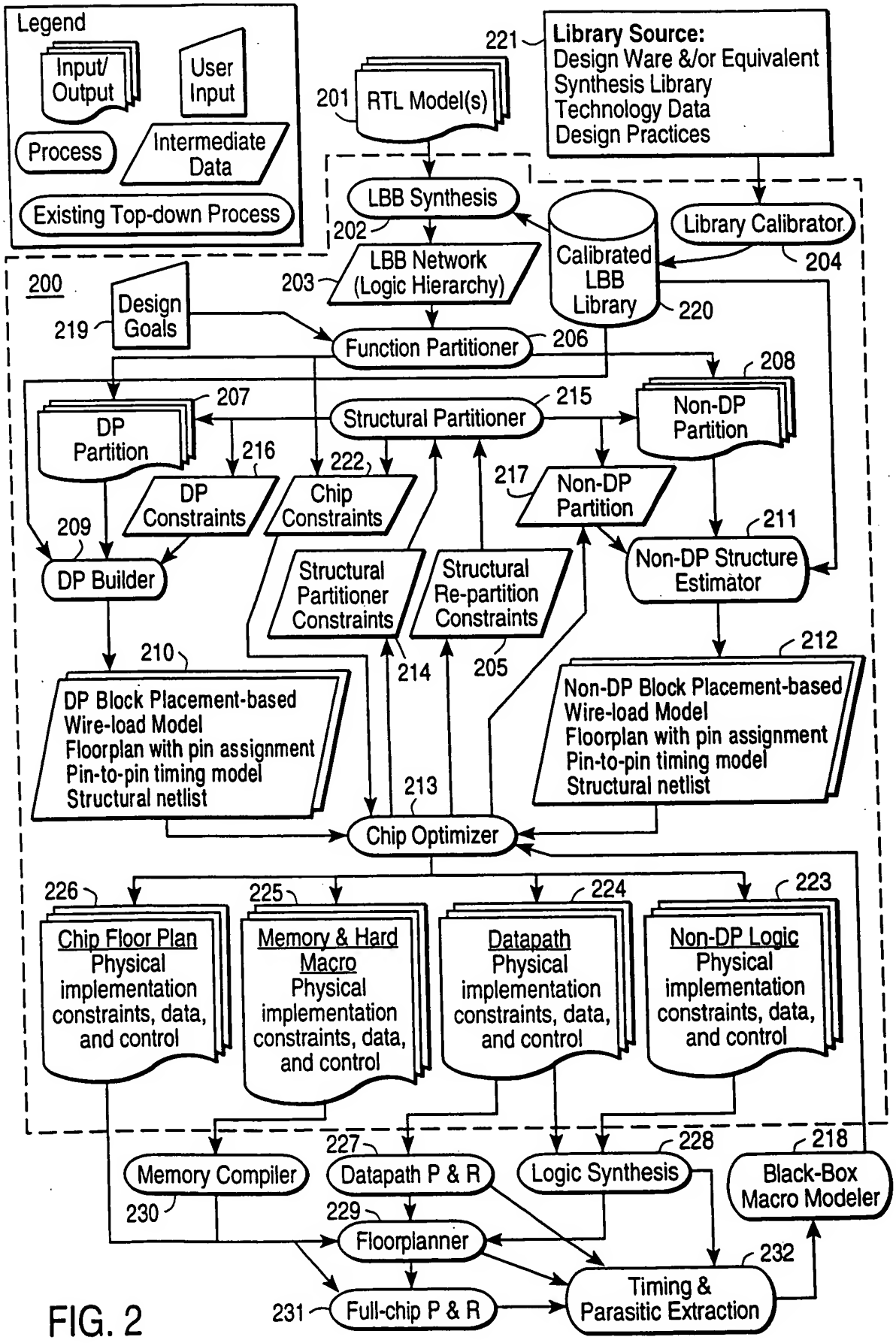


FIG. 2

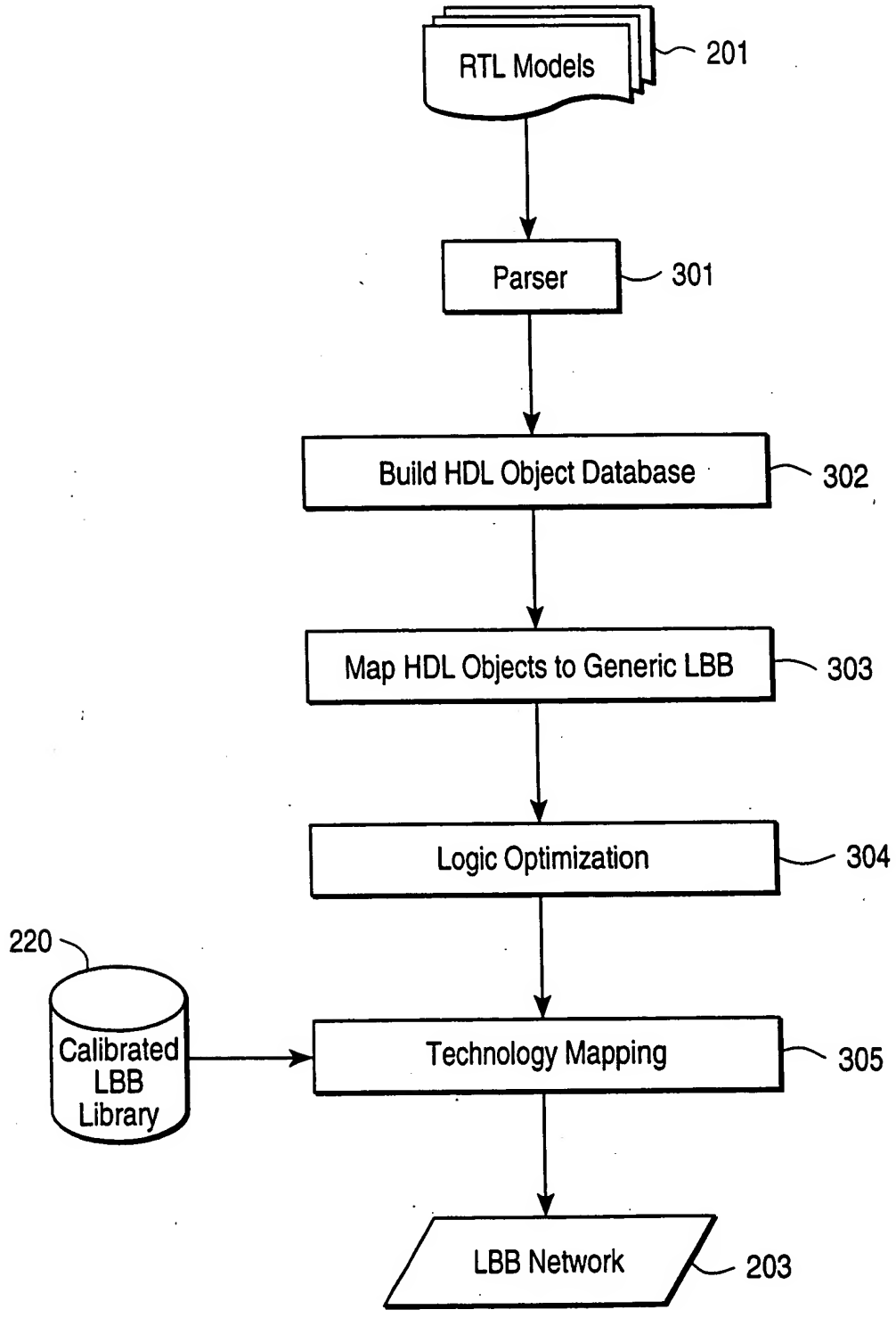


FIG. 3

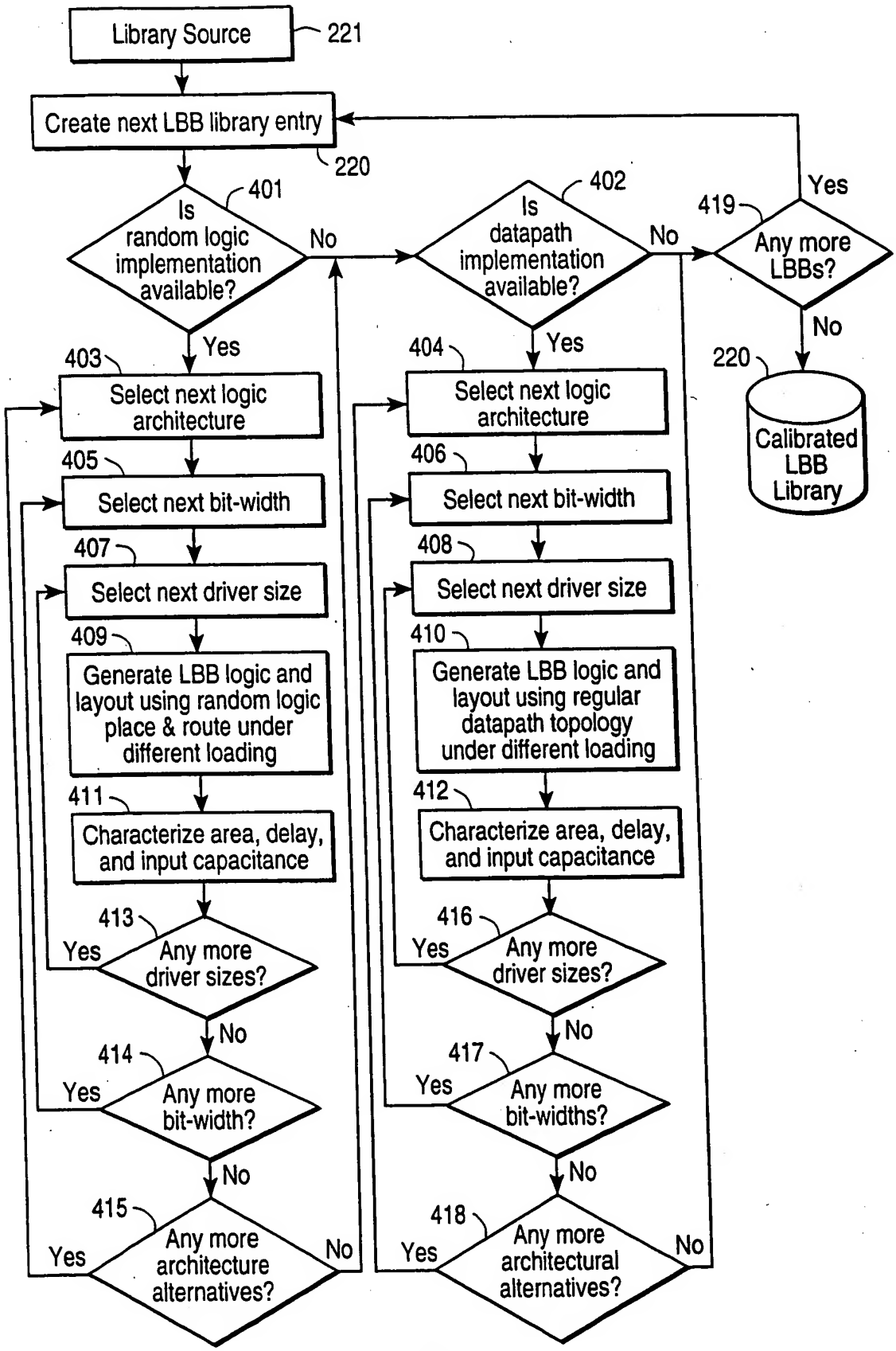


FIG. 4

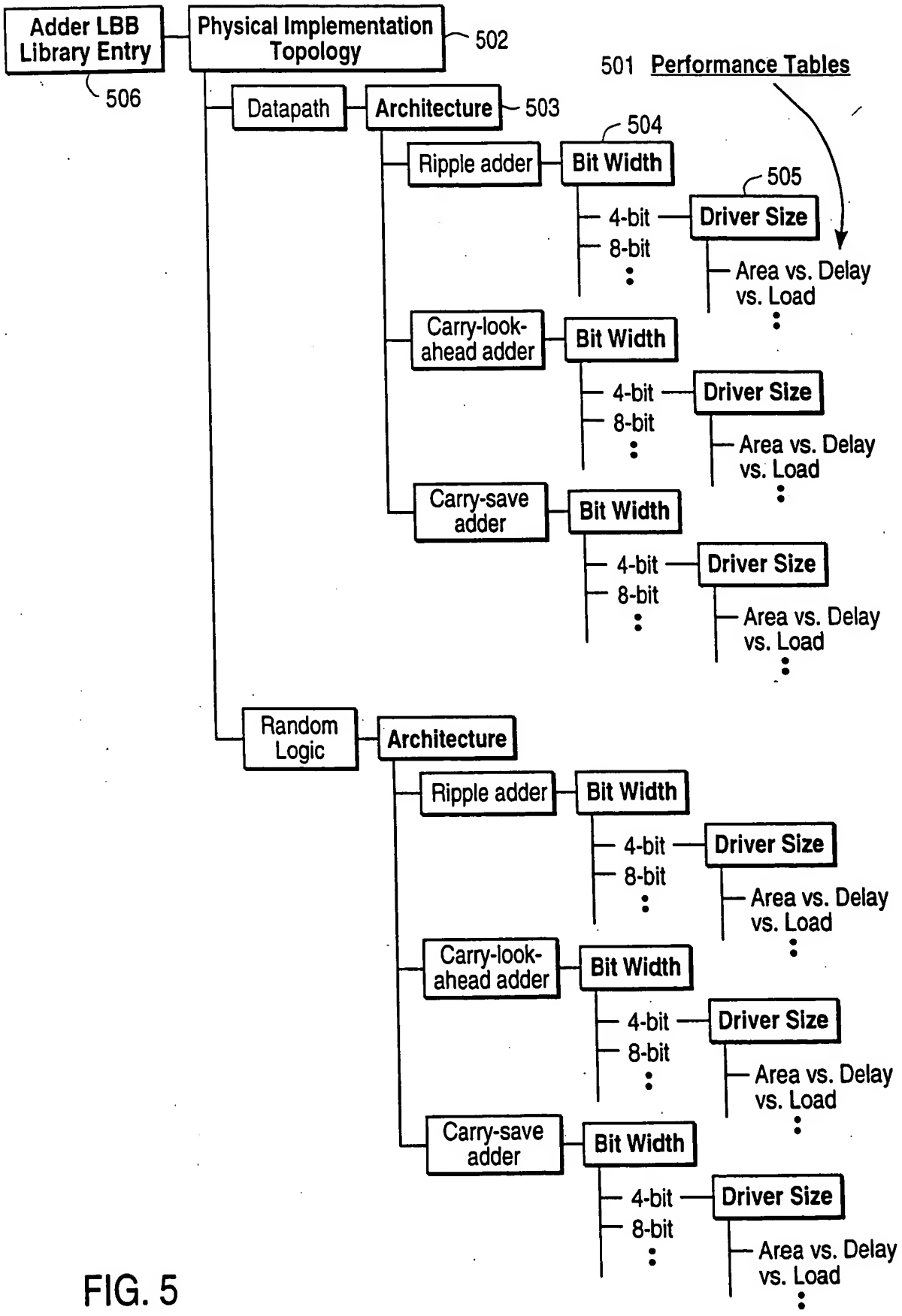


FIG. 5

Category	LBB
Adder	Adder, AdderCi, AdderCiCo, AdderCo
Arithmetic	ALU, Modulus, Multiplier, Divider, UnaryMinus
Buffers	Buffer, TriStateBuf
Comparator	Equal, Greater, GreaterOrEqual, Less, LessOrEqual, NotEqual
Complex Logic	Finite State Machine, Hard Macros
Decoder	BinaryDecoder
Decrementer	Decrementer, DecrementerCi, DecrementerCiCo, DecrementerCo
Encoder	BinaryEncoder, PriorityEncoder
Incrementer	Incrementer, IncrementerCi, IncrementerCiCo, IncrementerCo
Logic Gates	And, Nand, Nor, Or, Xnor, Xor, Inverter, And-Or (AO), And-Or-Invert (AOI)
Memory	RAM, ROM, Register File
Mux	Mux, PriorityMux, UnencodedMux (AOI), InvMux, InvPriorityMux, InvUnencodedMux
Reduce Gates	ReduceAnd, ReduceNand, ReduceNor, ReduceOr, ReduceXnor, ReduceXor
Shift	ArithmeticShift, CircularLeftShift, CircularRightShift, ShiftLeft, ShiftRight
Storage	Latch, FlipFlop
Subtractor	Subtractor, SubtractorCi, SubtractorCiCo, SubtractorCo

FIG. 6

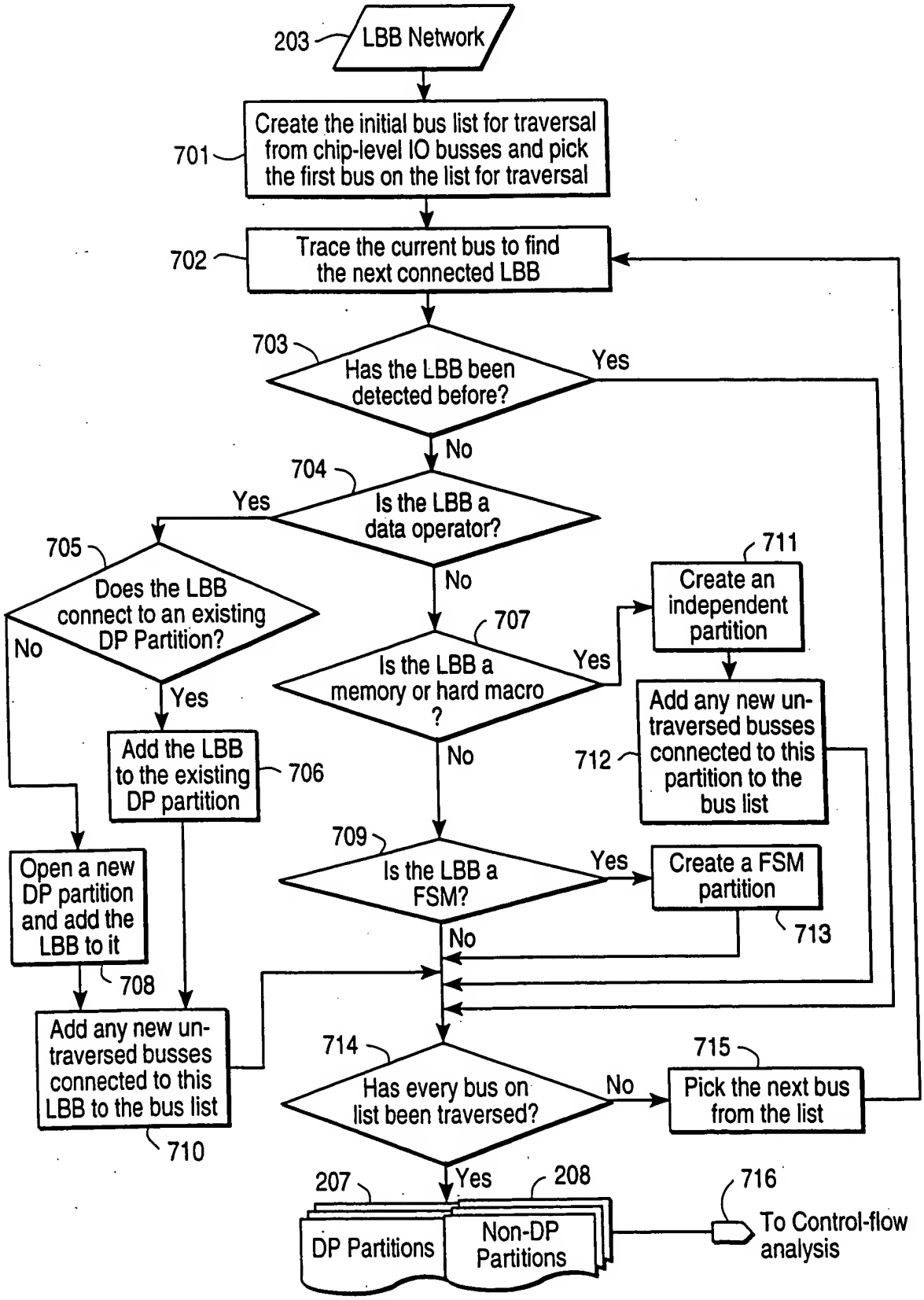


FIG. 7

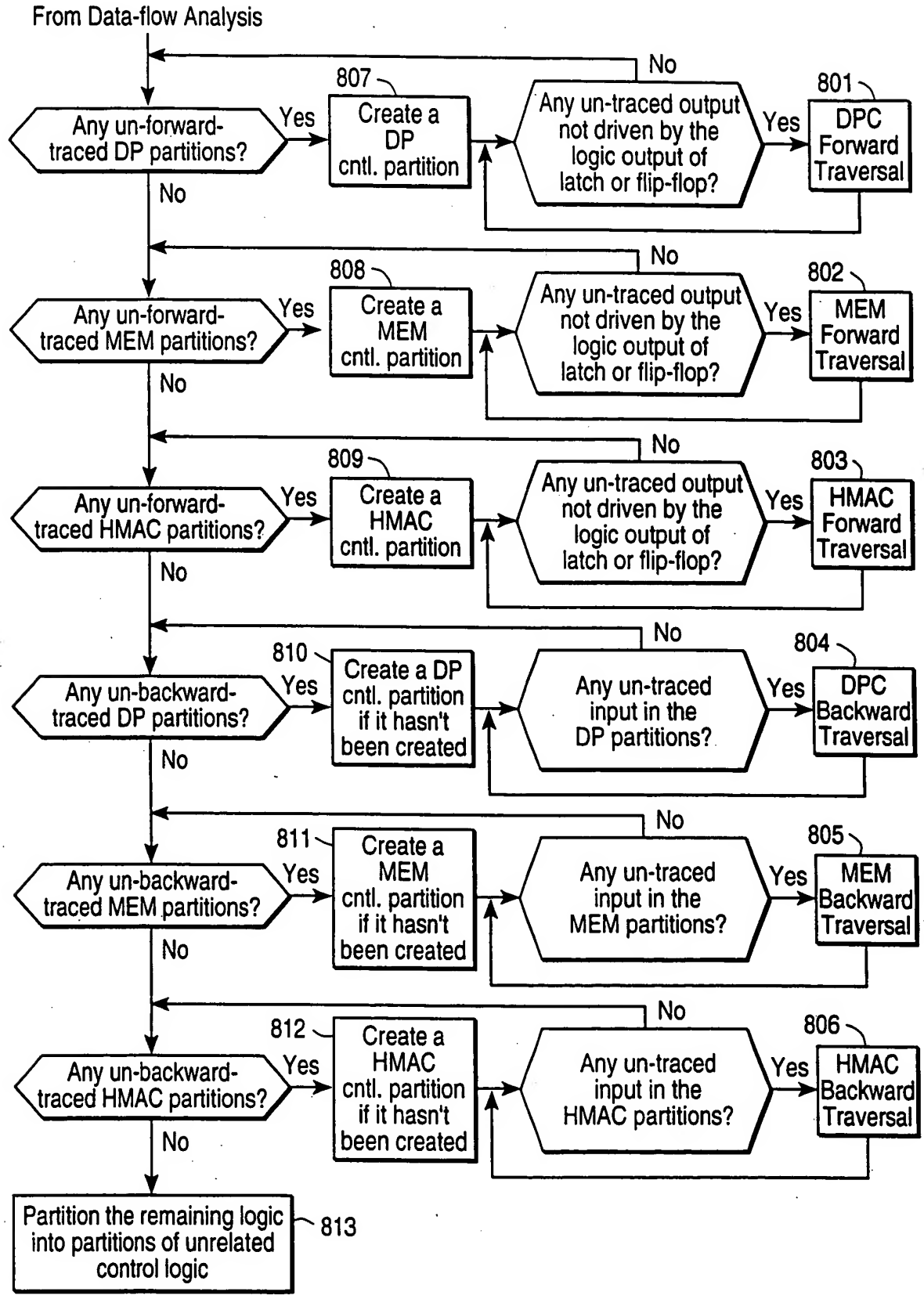


FIG. 8

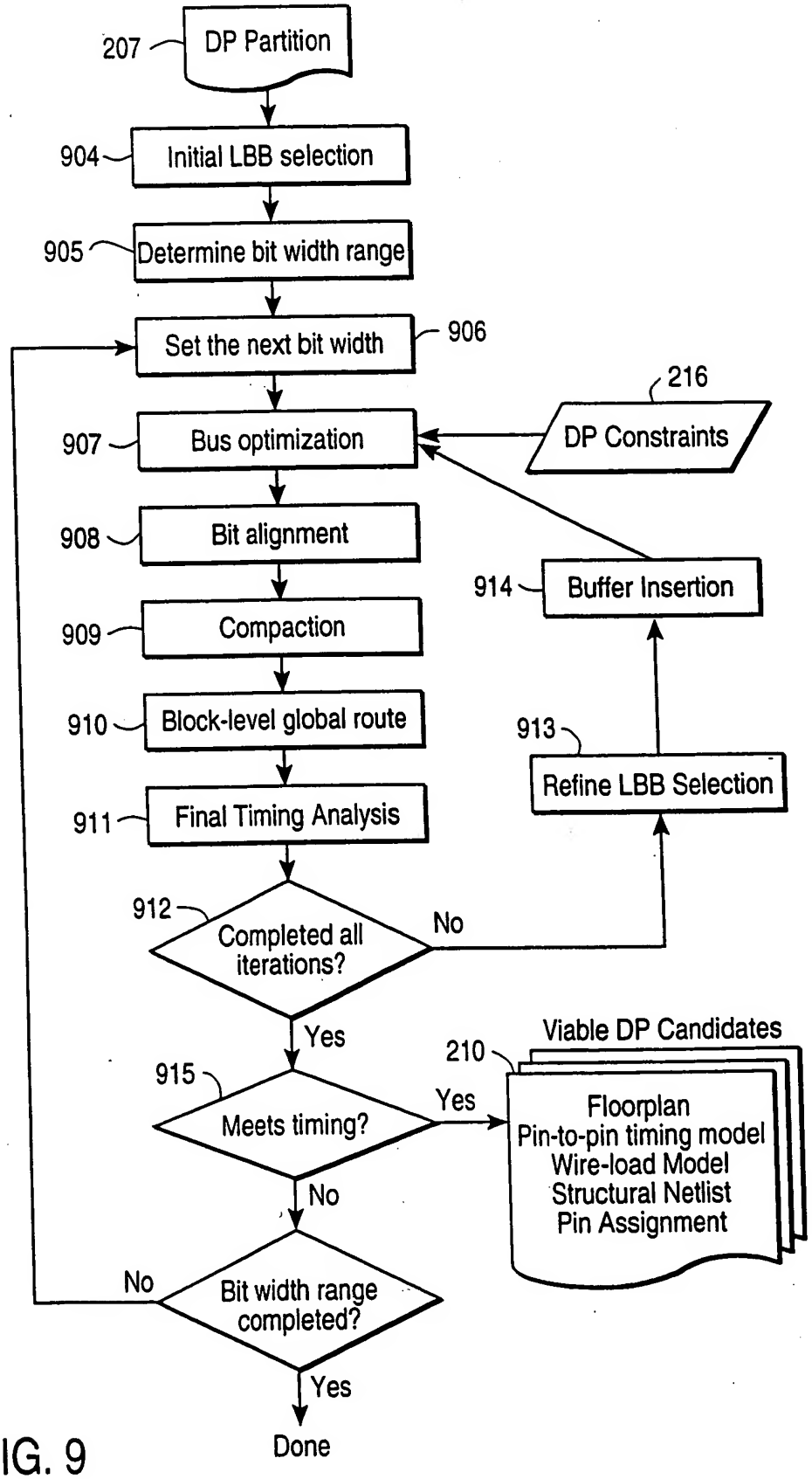
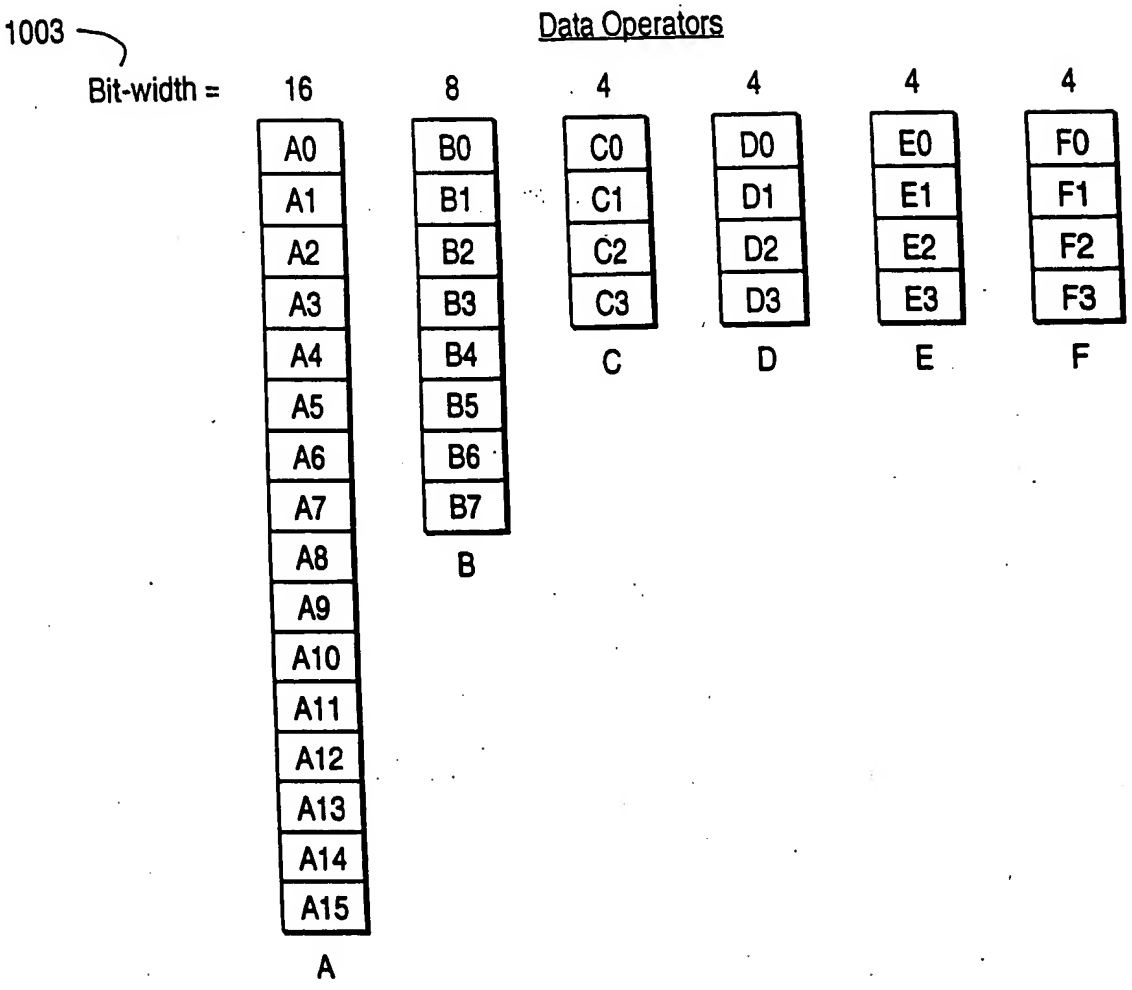


FIG. 9



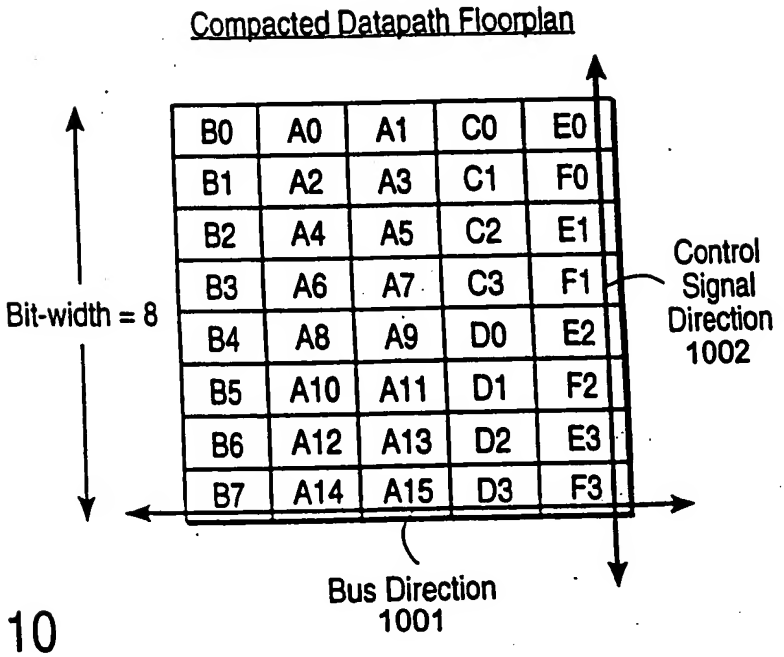


FIG. 10

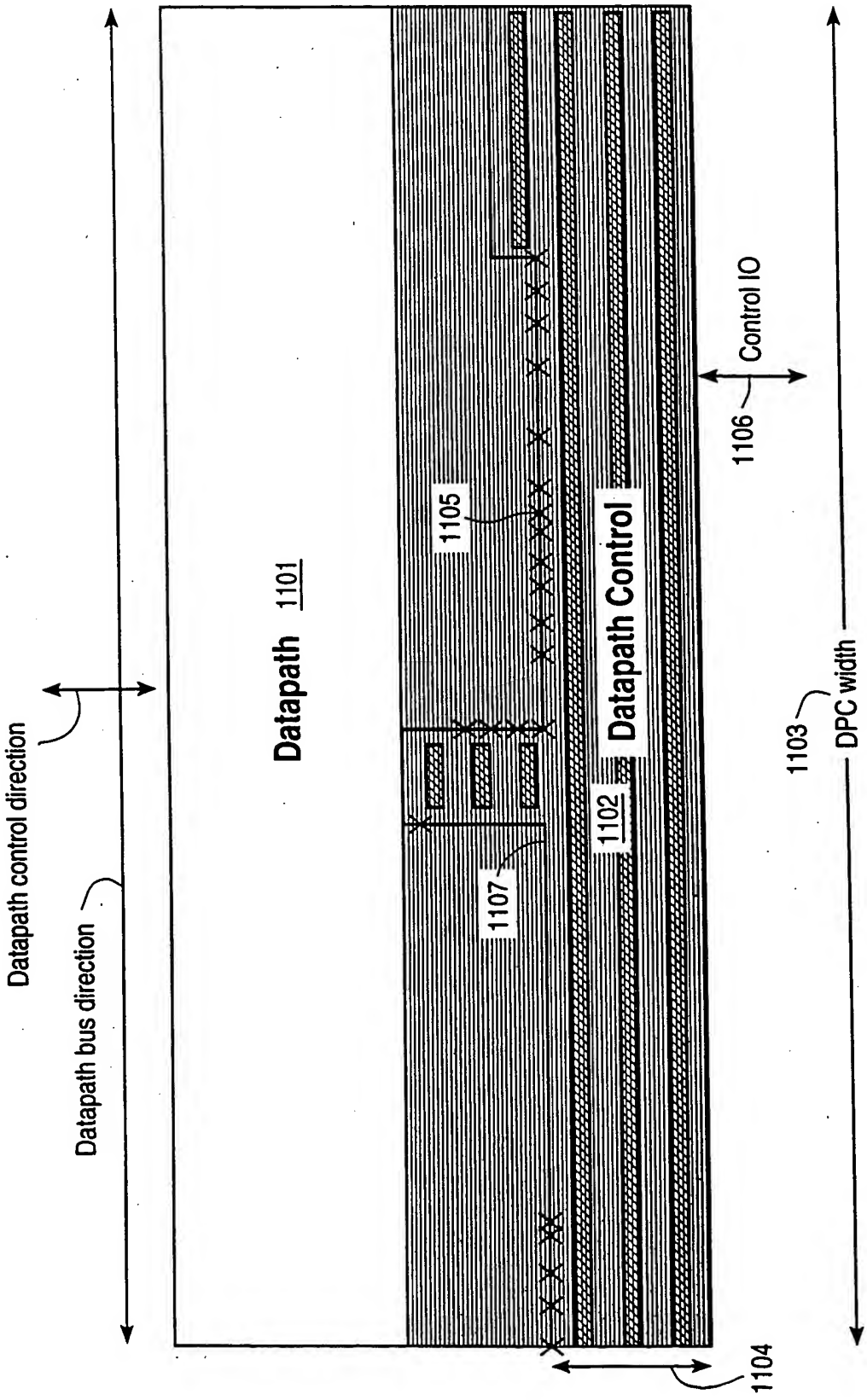


FIG. 11

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Atty. Docket No.: 21192-06625
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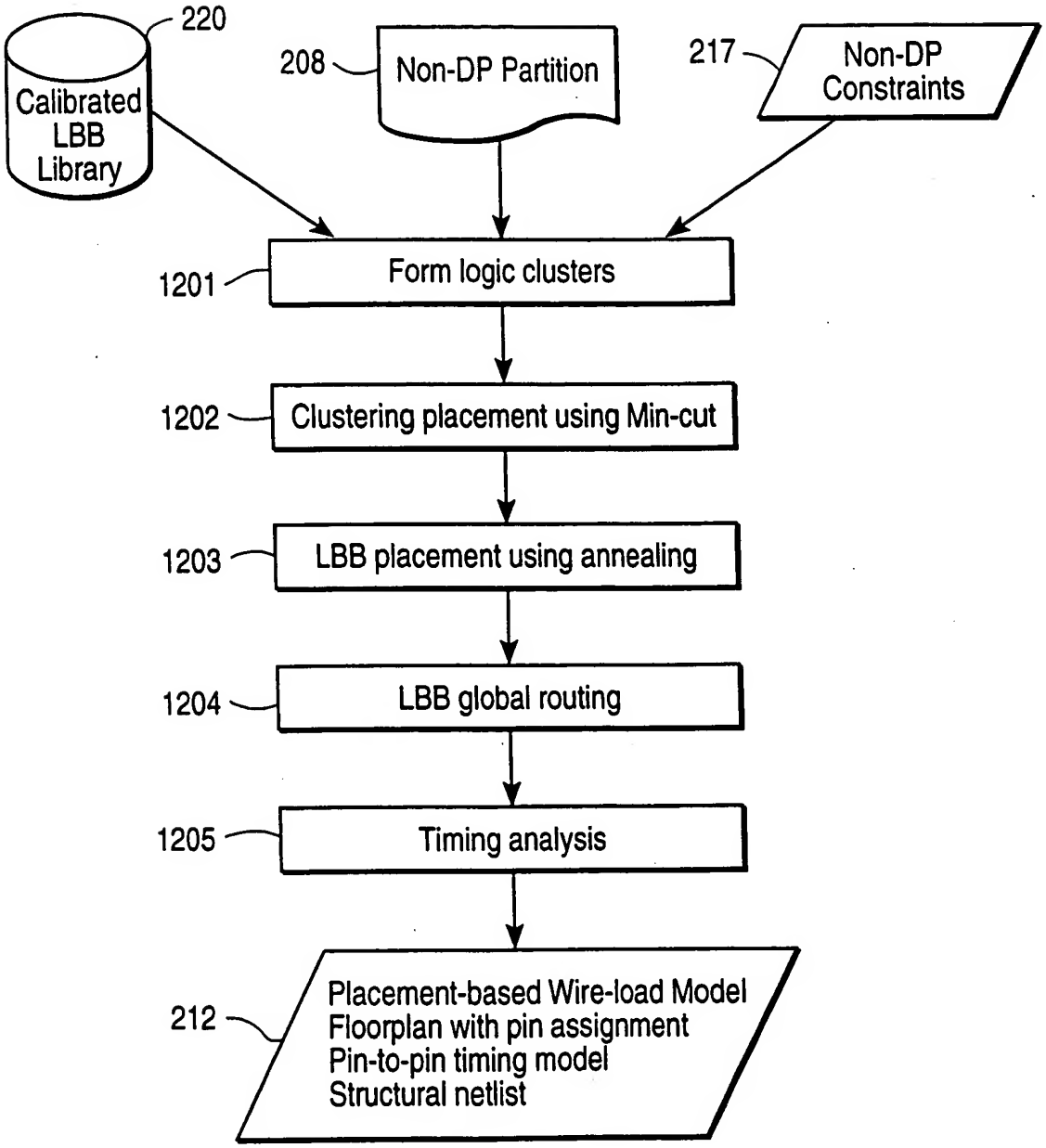

FIG. 12

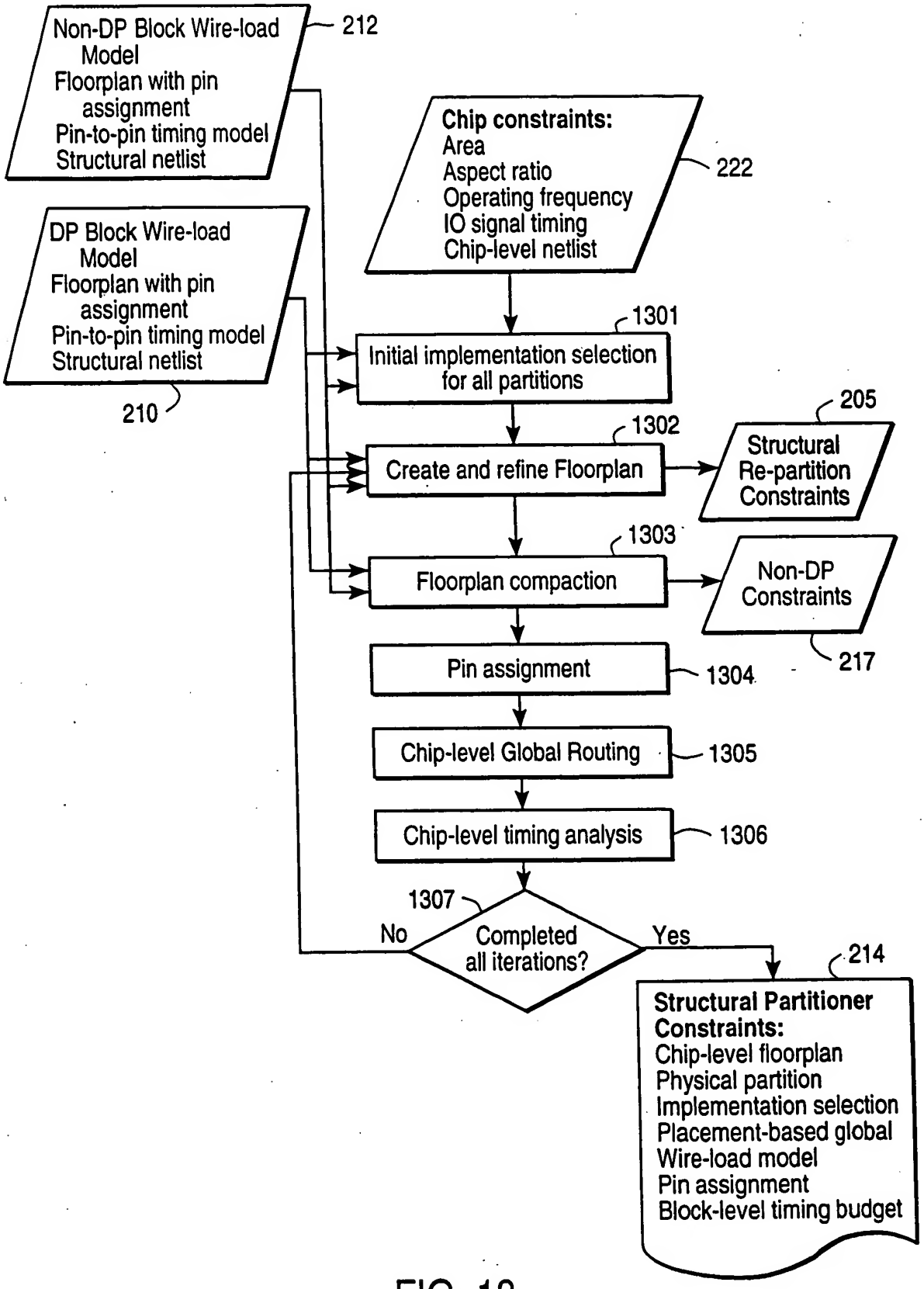

FIG. 13

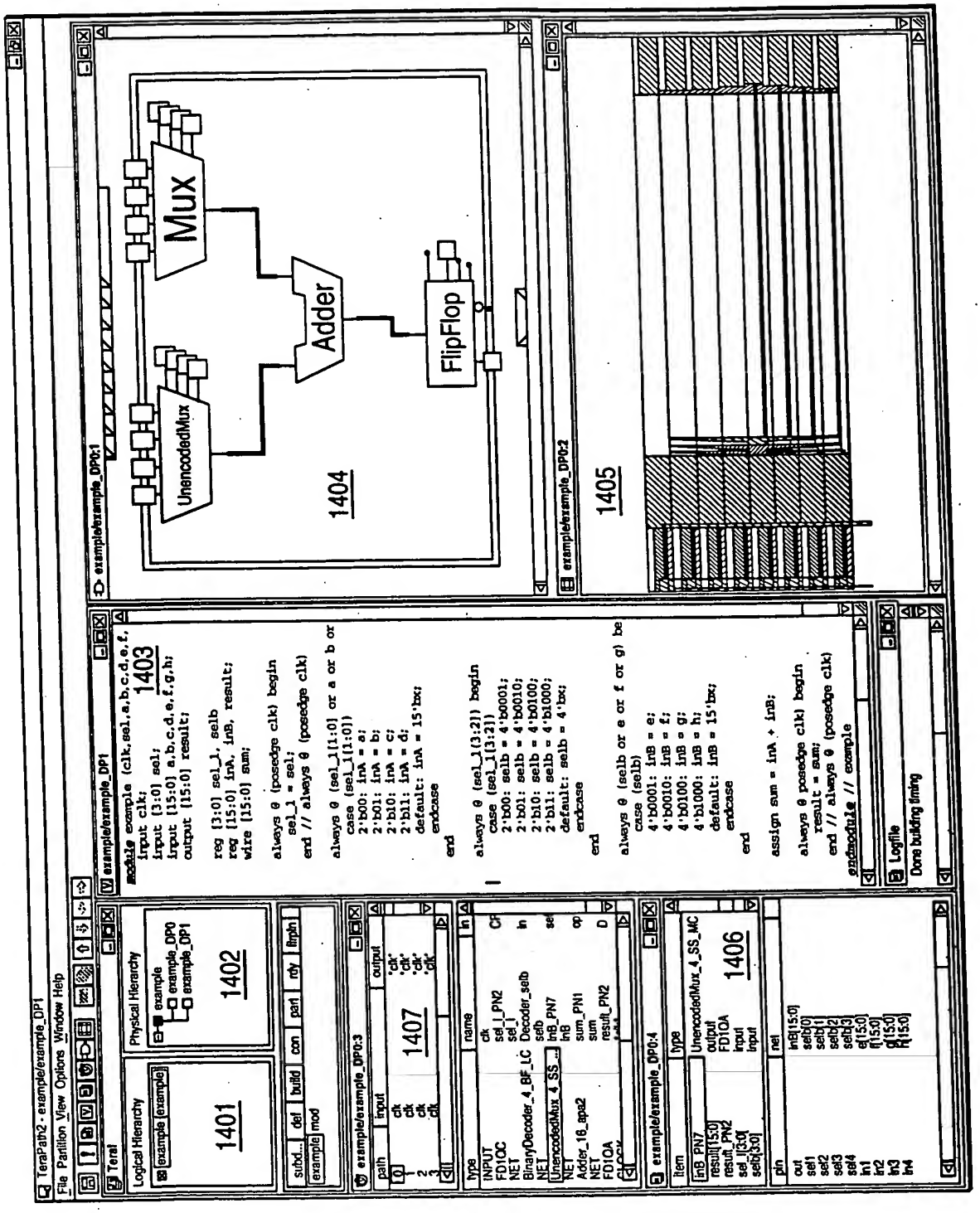

FIG. 14